

In re DAVID GLEN ROE, Application No. 09/814,244
Amendment D

REMARKS

In response to the non-final Office action mailed December 3, 2003, please consider the amendments and remarks presented herein. Reconsideration and/or further prosecution of the application is respectfully requested. No new matter is added herein.

In order to further the prosecution of this case as four non-final Office actions have been mailed in this matter, applicant has amended the pending claims to limit the issues and as such, all presently pending claims are believed to be allowable, as they are neither taught nor suggested by the prior art.

Claims 15-20 are canceled herein without prejudice, and applicants reserve the right to represent in this or a continuation case.

In regards to the previously pending claim set of claims 1-8, claim 1 is amended herein to roughly include the limitations of previously pending claims 1, 3, 4/6/7 (same limitation), and 5, with the limitation of claim 3 changed to recite that the buffer is electrically *coupled to* the off-chip reference clock input and the buffered reference clock output instead of *between*. Claims 3-7 are canceled herein. Thus, currently amended claims 1, 2, and 8 are pending.

Similarly, in regards to the previously pending claim set of claims 9-14, claim 9 is amended herein to roughly include the limitations of previously pending claims 9, 11/13, and 12 (same limitation). Claims 11-13 are canceled. Thus, currently amended claims 9, 10 and 14 are pending. Also, claim 9 is amended to recite that the means for buffering is electrically coupled to (instead of between) the off-chip reference clock input and the buffered reference clock output.

Thus, pending independent claims 1 and 9 include limitations of each being an applications-specific circuit (ASIC), with the first and second phase-locked loop circuit/circuit means being defined in one or more predefined libraries with the second phase-locked loop circuit/circuit means being specified to being connected to an output of a receiver on the ASIC, and the buffer / means for buffering connected to (not just between) the off-chip reference clock input and the buffered reference clock output.

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The Office action rejected the pending claims/limitations of claims 1 and 9 based on being anticipated by Sugawara (JP 10135786), and being obvious based on Sugawara and Yabe et al., US Patent 5,698,876.

First, these rejections of the ASIC limitation (original claims 5 and 12) were rejected as being anticipated under 35 USC § 102 by Sugawara. Applicant respectfully traverses this rejection as these claims recite that the ASIC includes the first and second circuits/circuit means while the Sugawara specifically teaches at the end of the translated Abstract that device 19/20 is designed as a unit separate than PLL circuit 18, and thus it would not be possible that they are in a same ASIC as recited in original claims 5 and 12. For at least this reason, pending claims 1 and 9 incorporating the ASIC limitation are believed to be allowable.

Next, the definition of these circuits/circuit means (original claims 4, 6, 7, 11, and 13) in one or more predefined libraries of circuits was rejected as being obvious in the combination of Sugawara and Yabe et al. Applicant notes that pending claims 1 and 9 include the further limitation that the second phase-locked loop circuit/circuit means is *specified to be connected to an output of a receiver on the ASIC*, which is an additional and narrow limitation neither taught nor suggested by Sugawara nor Yabe et al. For at least this further reason, claims 1 and 9 are believed to be allowable.

Finally, the Office action relies on buffer 18g of Sugawara for teaching a buffer being electrically coupled between the off-chip reference clock input and the buffered reference clock output. Applicant notes that pending claims 1 and 9 include the further limitation that the buffer / means for buffering is connected *to* instead of *between* as previously recited in claims 3 and 9. It is clear from Fig. 2 of Sugawara that Sugawara neither teaches nor suggests this limitation. For at least this further reason, claims 1 and 9 are believed to be allowable.

Therefore, for at least one of these reasons and especially in light of the combination of all of these reasons and the additional limitations added herein to the independent claims, claims 1 and 9 and their pending dependent claims of 2 & 8 and 10 & 14 respectively are believed to be allowable, and applicant respectfully requests all pending claims be allowed.


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As such all pending claims are believed to be allowable, the application is considered in good and proper form for allowance, and the Office is respectfully requested to issue a timely Notice of allowance in this case. Applicants request any and all rejections and/or objections be withdrawn. If, in the opinion of the Office, a telephone conference would expedite the prosecution of the subject application, the Office is invited to call the undersigned attorney. The Commissioner is hereby generally authorized under 37 C.F.R. § 1.136(a)(3) to treat this communication or any future communication in this or any related application filed pursuant to 37 C.F.R. § 1.53 requiring an extension of time as incorporating a request therefore, and the Commissioner is hereby specifically authorized to charge Deposit Account No. 501430 for any fee that may be due in connection with such a request for an extension of time.

Respectfully submitted,
The Law Office of Kirk D. Williams

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By

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